

Fig. 1





Fig. 4 is a block diagram of a digital circuit 40. The circuit 40 includes a register 101, a set of XOR gates 103a-f, a set of AND gates 109a-f, a set of inverters 105a-e, and a set of multiplexers 107a-e. The register 101 has inputs D, C, and R, and output Q. The circuit 40 is divided into two main sections by a dashed line 42. The left section contains the register 101 and the first two multiplexers 107a and 107b. The right section contains the remaining logic blocks. The circuit 40 has inputs Clock, Reset, and DATA IN (0, 31, 30, 29, 28, 27, 26, 25:1). It has outputs DATA OUT (31, 30, 29, 28, 27, 26:0). The circuit 40 is controlled by a signal 44.

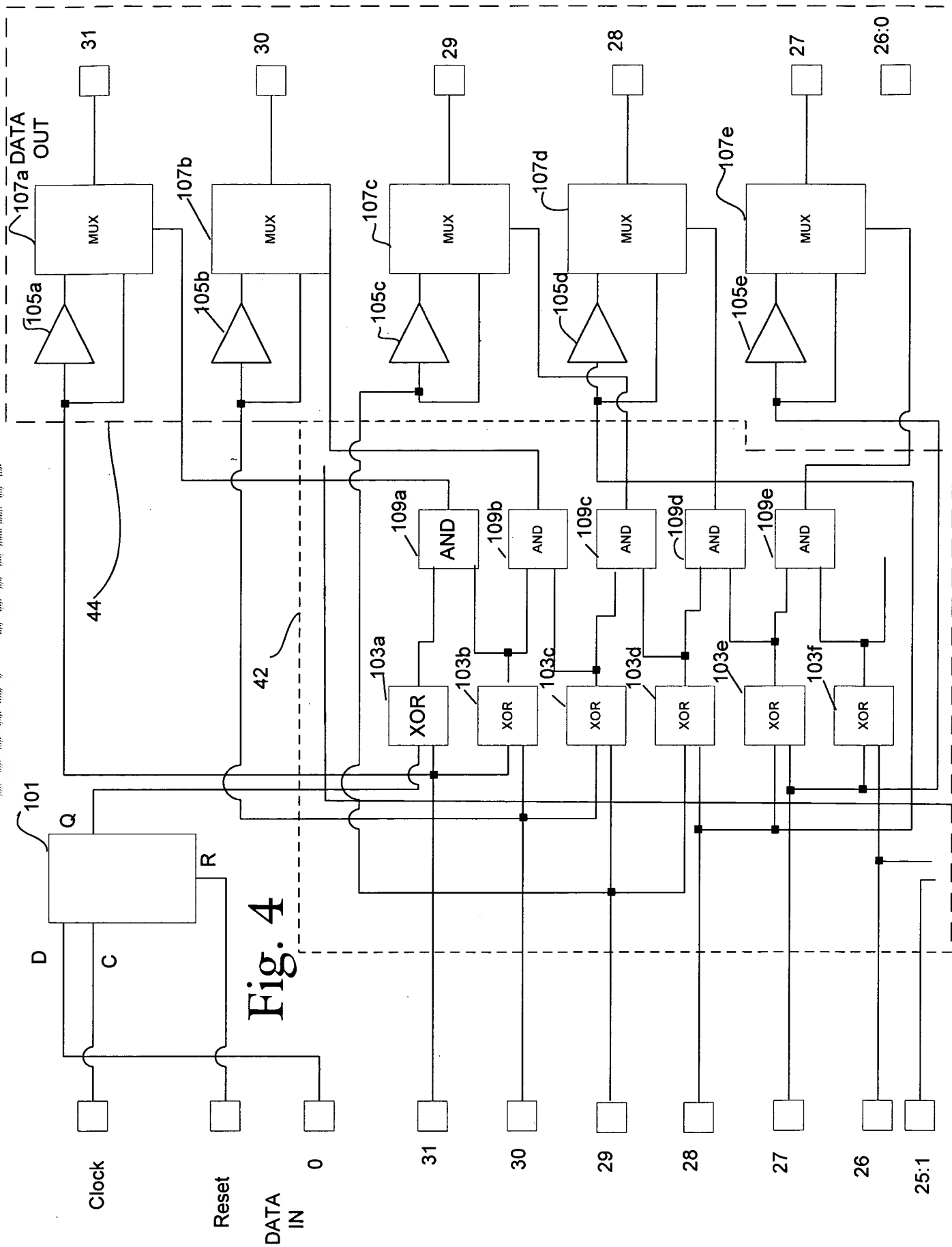


Fig. 4

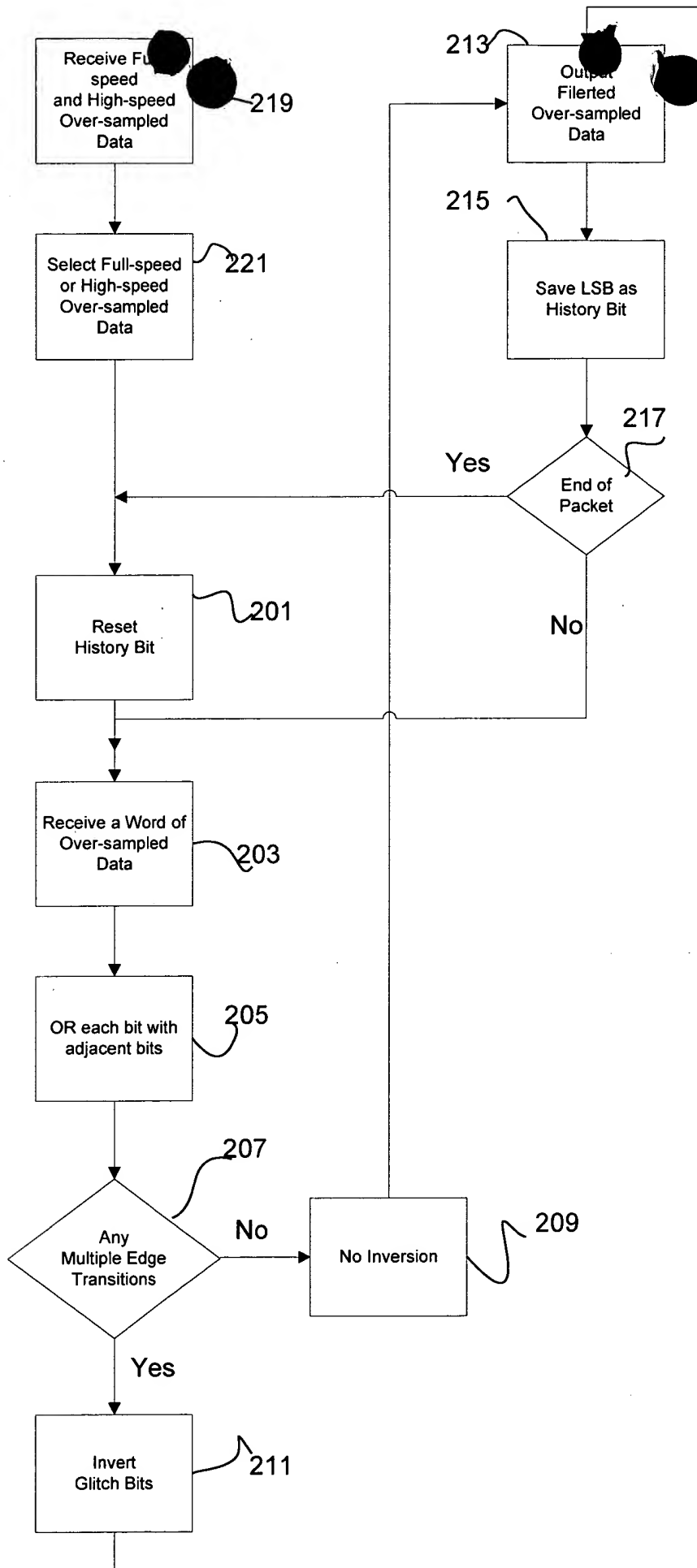


Fig. 5